

Rapid thermal annealing in silicon diode and photodiode technologies

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Abstract

The effect of rapid thermal annealing in H₂ atmosphere on the ohmic properties of contacts on the basis of two-layered transition metals (e.g. Ti, Ni, Pd and Cr) and Au compositions on p⁺-Si has been studied. It has been shown for the example of two-layered Ti/Au compositions that rapid thermal annealing in H₂ atmosphere at 340 °C for 20 s provides for an ohmic contact with lowest specific resistivity due to the formation of silicides at the Si/Me interface (Me = Ti, Ni, Pd and Cr). The applicability of the process in silicon diode technology for reducing the series resistance and increasing the device yield has been confirmed for small contact area commercial p⁺-n clamping diodes. Furthermore, the effect of rapid thermal annealing in H₂ atmosphere on the level of reverse dark currents in highly ohmic p-Si photodiode has been studied. The results for the commercial p-i-n silicon multi-pad photocells suggest an improvement of the dark currents of the photosensitive pads and the guard ring after rapid thermal annealing in H₂ atmosphere at 450 °C for 5 s and an increase in the device yield. This can be attributed to the hydrogen saturation of the dangling silicon bonds, providing for a decrease in the density of the surface states and stabilization of the charge properties at the SiO₂/p-Si interface. The applicability of rapid thermal annealing in H₂ atmosphere for dark current reduction in highly ohmic p-Si photodiode technology has been confirmed.

Keywords

rapid thermal annealing, RTA, ohmic contact, Si/Me interface, SiO₂/p-Si interface, photocell

1. Introduction

Low contact resistance ρ_s is a key requirement to the design of ohmic contacts, along with endurance and stability under severe operation conditions. However, an increase in the resistivity at the silicon/metal interface is unavoidable. The latter can be caused by either silicon surface treatment quality before metallization or the structure of the forming metallization layer and the charge properties at the Si/Me interface. Furthermore, the surface of silicon

always has a natural oxide layer which directly affects the properties of the contact due to mechanical stress. Moreover, the formation of complex metallic phases whose resistivity is often higher than that of the raw components of the metallization increases the overall contact resistance.

Transition metal silicides, e.g. Me = Ti, Ni, Pd and Cr, have a low resistivity and thermal compatibility with silicon [1, 2], making them promising candidates for the fabrication of ohmic contacts. There is the assumption that rapid thermal annealing (RTA) in an H₂ atmosphere

can fundamentally improve the properties of contacts to p^+ -Si due to the formation of the abovementioned silicides at the Si/Me interface. Moreover, this favors the purification of the silicon interface at an atomic level [3], thus further reducing the contribution to the contact resistance.

The reverse dark current is an important parameter of photodiode structures. The contribution of the surface component to the dark current of highly ohmic p -Si photodiodes comes mainly from the surface states at the interface of silicon oxide SiO_2 , which is used as an insulating film, and from the semiconductor bulk itself. Thermally grown silicon oxide films are known to contain a positive built-in charge [4, 5]. Partial compensation of that positive charge stabilizes the charge properties at the SiO_2/p -Si interface. This can be achieved via hydrogen saturation of the dangling Si bonds [6], which reduces the density of the surface states at the SiO_2/p -Si interface. There is the assumption that RTA in an H_2 atmosphere can reduce the level of the reverse dark current of silicon photodiodes with silicon dioxide dielectric films due to a lower contribution of the surface component originating from the stabilization of the charge properties at the SiO_2/p -Si interface.

Presented below are data on the effect of RTA in an H_2 atmosphere on the properties of ohmic contacts for the example of a two-layered Ti/Au composition on p^+ -Si, as well as its effect on the reverse dark current of a p -Si photodiode with a SiO_2 dielectric film. Furthermore, the applicability of RTA in an H_2 atmosphere for silicon diode and photodiode structure technologies was evaluated.

2. LTLM measurement of specific contact resistance

The fabrication of ohmic contacts requires the capability to measure low specific resistances. There are a number of techniques and their modifications which are used for measuring the specific contact resistance of semiconductor structures. TLM (transmission line method) is one of the most widely used specific contact resistance measurement techniques which takes into account the spreading currents under the contact in the semiconductor bulk, due to the possibility of its adaptation to thin semiconductor films and diffusion layers. Generally, the basics of the technique are as follows. The specific contact resistance ρ_s is determined via probe measurements of the full contact resistance R_T between planar contact pads. The parameter R_T includes the contact resistance R_C and the semiconductor bulk resistance R_S [7]. Depending on the geometrical shape of the contact pads, the technique in question has two modifications: CTLM (circular transmission line method) and LTLM (linear transmission line method).

CTLM specific contact resistance measurement is described in detail in earlier works [8–11]. For example, the CTLM technique was used for studying the ohmic

behavior of $\text{Ti}/n^+\text{-ZnO}/n\text{-Ge}$ and $\text{Ti}/\text{ITO}/n\text{-Ge}$ MDS contacts [10]. Cr/Au, Cr/Au/Ag/Au, Ti/Pt/Au, Pt/Ti/Pt/Au, Pt/Au, Ti/Au, Ti/Pt/Ag and Ti/Pt/Ag/Au contact structures on p -GaSb were studied for the fabrication of high photocurrent density photocells (to 15 A/cm^2) [11]. The LTLM technique was described elsewhere [12, 13]. Current propagation mechanisms in Pd/Ni ohmic contacts to p -GaN were studied and optimum metallization layer thickness ratio with minimum specific contact resistance were determined [12]. The contact properties of multilayered Ti (0.02 mm)/Au (0.06 mm)/Pd (0.04 mm)/Au (0.05 mm) metallization on n -GaN were studied [13].

The LTLM technique with linear semiconductor contacts was used in this work. LTLM measurements were conducted for test structures consisting of multiple similar rectangular contact pads with the length A and the width Z , having different distances between one another, i.e., L_{12} , L_{13} , L_{23} etc. [14]. Minimization of the edge current spreading contribution requires the condition $Z \ll A$ be met.

The specific contact resistance is determined via probe measurements of the resistance between the contact pads and plotting a resistance vs contact pad spacing graph (Fig. 1), whose tilt angle is R_S/A , with L_T being the transmission length.

Linear approximation of the measured resistance vs contact pad spacing curve allows determining the specific contact resistance using the following equations:

$$R_T = 2R_C + R_S \left(\frac{L}{Z} \right); \quad (1)$$

$$\rho_C = \frac{R_C^2 Z^2}{R_S}, \quad (2)$$

where R_C is the contact resistance; R_S is the semiconductor bulk resistance; L is the contact pad spacing; Z is the contact pad width.

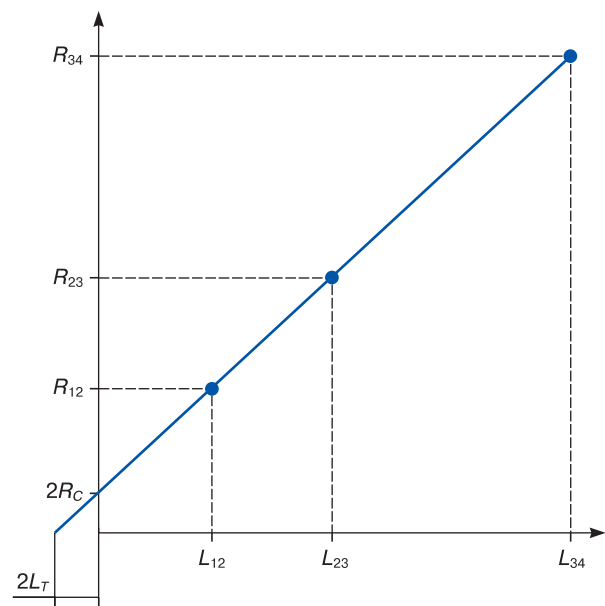


Figure 1. LTLM measurement of specific contact resistance

Table 1. Distance between contact pads of test structures

#	Contact pads	Distance (mm)	#	Contact pads	Distance (mm)	#	Contact pads	Distance (mm)
1	L_{12}	10	6	L_{23}	20	11	L_{35}	170
2	L_{13}	130	7	L_{24}	150	12	L_{36}	320
3	L_{14}	230	8	L_{25}	290	13	L_{45}	40
4	L_{15}	400	9	L_{26}	440	14	L_{46}	190
5	L_{16}	550	10	L_{34}	30	15	L_{56}	50

3. Test structures and experimental technique

The studies were carried out for 60 mm *n*-Si wafers. The wafers were chemically pretreated in an ammonia-peroxide solution and boron doped by means of 100 keV accelerated ion implantation at a $6.0 \cdot 10^{14} \text{ cm}^{-2}$ dose for producing a heavily doped p^+ surface region.

The LTLM contacts were fabricated by vacuum deposition of a two-layered composition, i.e., gold with an adhesive titanium sublayer, followed by photolithographic stripping of similar rectangular pads with 10 to 550 mm distance from one another (Table 1). The contact pad sizes were $100 \times 1000 \text{ mm}^2$.

The thickness of the Au layer was 0.5 mm, and that of the adhesive Ti sublayer, 0.02 mm. The metallization thickness was measured with a Bruker Dektak 3030 contact profilometer.

Then the test structures were subjected to RTA in an H_2 atmosphere. The heat treatment temperature should be far below the melting points of the metals used in the contact: $t_{\text{mAu}} = 1337^\circ\text{C}$ and $t_{\text{mTi}} = 1668^\circ\text{C}$ [14, 15]. Thus, the following RTA temperatures were used: 300, 320, 340 and 360°C . The RTA time also differed: 10, 20 and 30 s. The test structures after RTA at 360°C for 10 s had initial signs of Au film exfoliation from the Ti sublayer, probably due to the difference in the coefficients of linear thermal expansion α (CLTA) of Au and Ti by almost 1.5 times: α_{Au} is $(13.3\text{--}14.5) \cdot 10^{-6} \text{ K}^{-1}$, while α_{Ti} is $(7.23\text{--}8.82) \cdot 10^{-6} \text{ K}^{-1}$ [15–17]. Nevertheless, the above test structures were also studied.

RTA was carried out in an RSO-650-200 NPO high-temperature vacuum melting furnace having 18 IR lamps 18 kW each and designed for the 50 to 650°C range and a high heating rate (above 75°C/s).

4. Results and discussion

The electrophysical parameters of the test structures were probe-measured with a Hewlett Packard 4277ALCZ meter in the -50 to 50 V range. The test structure measurements were carried out twice: immediately after the formation of the two-layered Ti/Au metallization and after RTA. Comparison between the typical current-voltage characteristics of the test structures before and after RTA

in an H_2 atmosphere at different temperatures for different time is shown in Fig. 2.

The data (see Fig. 2) suggest that immediately after the formation of the two-layered metallization, the current-voltage characteristics of all the test structures were nonlinear, even at low voltages, and RTA at 300 and 320°C did not bring any significant improvement to the contact properties of the test structures. Linear and symmetrical current-voltage characteristics are achieved after RTA at 340°C for 10 s or longer. Further increase in the heat treatment temperature to 360°C provides for linear and symmetric current-voltage characteristics, despite Au film exfoliation from the adhesive Ti sublayer. Typical current-voltage characteristic before and after RTA in different modes are shown in Fig. 2. The optimum H_2 atmosphere RTA which is sufficient for the formation of an ohmic Ti/Au contact with p^+ silicon was chosen to be 340°C .

The time of RTA in an H_2 atmosphere at 340°C providing for an ohmic contact with the lowest specific contact resistance was found using the LTLM technique. Test structure measurements with the above technique and calculations using Eqs (1) and (2) yielded the following average specific contact resistances:

- RTA for 10 s: $9 \cdot 10^{-3} \text{ Ohm} \cdot \text{cm}^2$;
- RTA for 20 s: $7 \cdot 10^{-3} \text{ Ohm} \cdot \text{cm}^2$;
- RTA for 30 s: $7 \cdot 10^{-3} \text{ Ohm} \cdot \text{cm}^2$.

One can conclude that RTA in an H_2 atmosphere is an effective tool for fabricating ohmic contacts between two-layered Ti/Au compositions and p^+ -silicon. The mechanism of the observed process is as follows. Pulsed thermal annealing triggers the formation of titanium silicides at the Si/Ti interface, thus reducing the specific contact resistance. In this case, Ti can be replaced for other transition metals like Ni, Pd or Cr, since they also tend to form silicides upon interaction with silicon [1, 2].

4.1. p^+ -*n* clamping diodes

We consider the effect of RTA on the series resistance of the diode. The series resistance of a p - n junction is composed of the resistances of the n and p regions and the contacts to them [18]. Typically, the resistances of the n and p regions can be reduced by selecting optimum thicknesses of the regions and impurity concentrations therein. The contact resistances to the n and p regions depend on the materials used for metallization and the metallization

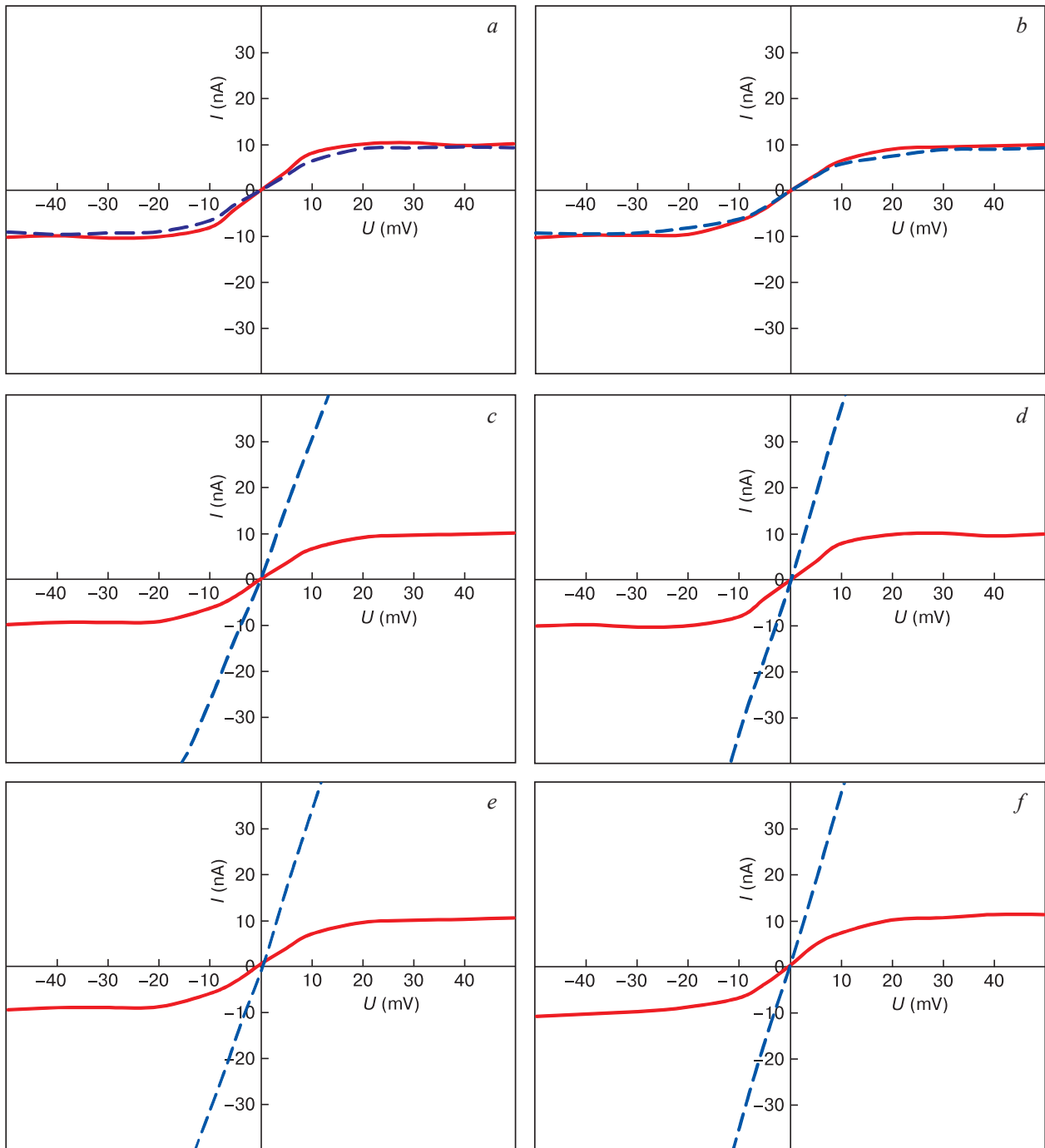


Figure 2. Typical current-voltage characteristics of test structures before and after RTA in H_2 atmosphere: (a, b, e) 300, 320 and 340 °C for 30 s, (c, f) 340 and 360 °C for 10 s, and (d) 340 °C for 20 s. Solid: after metallization formation; dashed: after RTA

formation technique. Aluminum can be used for the fabrication of ohmic contacts in the silicon device technology. The formation of aluminum contacts includes aluminum deposition to a thickness of about 1 nm, photolithographic stripping of contact pads and contact burning at 470–550 °C [19]. A disadvantage of aluminum in the ohmic contact technology is its failure to meet a number of environment impact endurance requirements.

High-endurance device technology requires the use of multilayered contact structures. Chromium, titanium, molybdenum and nickel can be used for adhesive sublayer fabrication. However, titanium is most widely

used due to its good adhesion to silicon and SiO_2 , ability to reduce SiO_2 by analogy with aluminum and absence of tendency to form intermetallic compounds [20]. The conductive layer deposited on the adhesive one should have a low resistivity and provide for good connection of gold outer contact wires. Gold meets all the above conditions.

The effect of RTA on the contact resistance of the diodes and the applicability of the technique for silicon diode technology were studied by measuring the parameters of four test batches of p^+-n clamping diodes with low p^+ region contact pad areas, i.e., 0.002 mm².

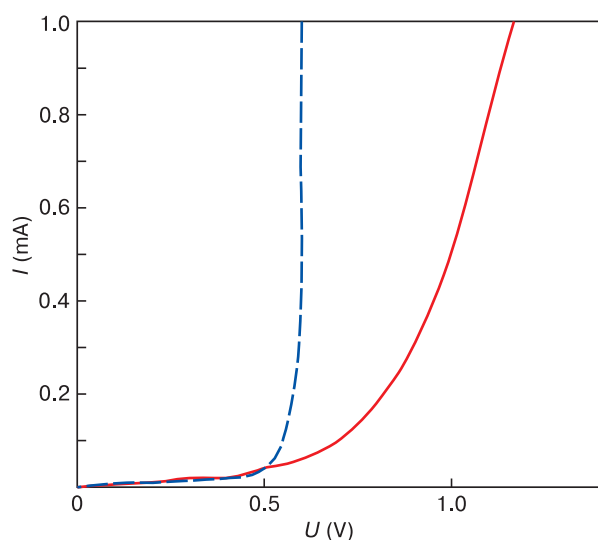


Figure 3. Typical forward branches of current-voltage characteristic of a p^+-n clamping diode. Solid curve: clamping diode without rapid thermal annealing (RTA); dashed curve: with RTA

Table 2. Typical series resistances of p^+-n clamp diodes

Parameter	Diodes	
	Conventional technology	RTA
Series resistance (kOhm)	1.2–1.3	0.6–0.7
Yield (%)	75	90

The raw materials for the above test structures were epitaxial 60 mm (100) n/n^+ silicon wafers, Grade 50KEF150/380KES0.01. The clamping diode technology also included an n^+ clamping region. Structure cross-section is illustrated in Patent [21].

The first and second clamping diode batches were fabricated following a standard route containing the following key process stages:

- thermal oxidation for passivation film;
- phosphorus ion implantation predeposition onto wafer face side followed by impurity thermal drive-in diffusion for n^+ clamping region;
- phosphorus ion implantation predeposition onto wafer rear side followed by impurity thermal drive-in diffusion for n^+ rear contact layer;
- boron predeposition onto wafer face side for p^+ region;
- vacuum deposition of two-layered Ti/Au metallic contacts to diode emitter and n^+ rear contact layer followed by photolithographic stripping.

The third and fourth clamping diode batches were additionally subjected to RTA in an H_2 atmosphere at 340 °C for 20 s, since at longer RTA time the contact resistance does not change, as shown above.

The forward branches of the current-voltage characteristics for the test clamping diodes were probe measured as described above. The measurement voltage

range was 0 to 1.2 V. Figure 3 shows a comparison of 2 typical forward branches of the current-voltage characteristics for test clamping diodes fabricated with and without RTA.

Table 2 shows typical series resistances and device yield of clamping diodes fabricated using conventional technology and modified route.

The results (Table 2) suggest that the use of RTA in an H_2 atmosphere at 340 °C for 20 s for the formation of an ohmic Ti/Au contact to p^+ -Si reduces the typical range of series resistances r_s . The lower limit of the range decreased twofold, and the upper, by 1.86 times as compared to those of the diodes fabricated following the conventional technology. In the meantime, the series resistances range for the RTA-treated diodes fully complies with the requirements to the clamping diodes in question, i.e., $r_s \leq 0.8$ kOhm. Thus, the device yield was increased by 15%. This confirms the applicability of RTA for series resistance reduction in p^+ -Si diode technology.

A Russian Federation Patent was granted for the results [22].

4.2. Multi-pad $p-i-n$ photodiodes

The effect of RTA on the dark current of silicon photocells with SiO_2 insulating films and the applicability of the technique in photocell technology were studied for two test batches of multi-pad $p-i-n$ photodiodes. The raw materials were 60 mm single-crystal (100) p -Si wafers with a specific resistance of 5 kOhm·cm. The photocell technology included photosensitive pads (PP) distributed in 4 quadrants and a planar guard n^+-p junction. The 4 external and 4 internal pads were located inside 4 and 2 mm diam. concentric circles, respectively. The areas of the external and internal PP were 18 and 0.6 mm², respectively, the gap between the pads being 200 nm [23]. Thermal SiO_2 was used for photocell periphery passivation, PP isolation and antireflection coating. Structure cross-section was reported earlier [24].

The first photocell batch was fabricated following the conventional process route consisting of the following key stages:

- thermal oxidation for passivation film;
- phosphorus predeposition and drive-in diffusion for photocell and guard ring regions;
- phosphorus predeposition onto rear wafer side for gettering layer;
- getter stripping;
- boron drive-in diffusion for p^+ rear contact layer;
- SiO_2 antireflection film stripping down to semiconductor for contact windows.

The second photocell batch route additionally included RTA in an H_2 atmosphere. The RTA temperature should be, on the one hand, below the melting points of the metals used in the contact and, on the other, sufficient for the effective formation of silicon-hydrogen bonds. The chromium melting point is $t_{mCr} = 1877$ °C [15], and

that of gold t_{mAu} was shown above. Thus, the following modes were selected:

RTA Temperature (°C)	RTA Time (s)
340	20
400	20
450	5
470	5
500	5

The PP and guard ring dark currents of the test photocells were measured using a Karl Suss PM-5 multi-probe measuring system at a 200 V working voltage.

The photocells after RTA at 340 and 400 °C did not exhibit any significant dark currents, either in the photocell or in the guard ring, regardless of RTA time. At a 450–500 °C pulse heat treatment temperature, the dark current became lower. The most efficient reduction of the PP and guard ring dark currents was achieved after RTA at 450 °C for 5 s.

Table 3 summarizes typical dark currents of PP and guard rings at the photocell working voltage, for photocells fabricated following the conventional route and the those subjected to additional RTA at 450 °C for 5 s, as well as the photocell yield data.

The data (see Table 3) suggest that the use of RTA in an H_2 atmosphere at 450 °C for 5 s reduces the typical range of dark currents. The bottom limit of the dark currents for the external PP decreased by 1.5 times and for the internal PP, by 1.6 times, as compared to the respective parameters for the standard photocell technology. Thus, the device yield was increased by 15%, thus confirming the applicability of RTA for the technology of highly ohmic p -Si photodiodes with SiO_2 insulating film. One can assume that the dark currents become lower due to the hydrogen saturation of the dangling Si bonds, providing for a decrease in the density of the surface states and stabilization of the charge properties at the SiO_2/p -Si interface.

Conclusions

The effect of rapid thermal annealing in an H_2 atmosphere on the ohmic properties of contacts were studied

for the example of a two-layered Ti/Au composition on p^+ -Si. Test structures on n -Si with heavily doped p^+ surface region were fabricated. Similar rectangular contact pads with 10 to 550 nm spacing were fabricated on the test structures for LTLM measurement with a linear semiconductor contact geometry.

The electrophysical parameters of the test structures were measured over a wide range of voltage (–50 to 50 V) immediately after the formation of metallization and after RTA at 300–360 °C with a 20 °C step for determining the temperature at which the current-voltage characteristics of the contacts become linear and symmetrical. The pulse treatment time providing for the lowest specific contact resistance was found via LTLM calculations of the specific contact resistances of the test structures after RTA at the selected temperature for 10, 20 and 30 s.

It was shown that RTA in an H_2 atmosphere at 340 °C for 20 s provides for the lowest specific contact resistance of Ti/Au on p^+ -Si, i.e., $7 \cdot 10^{-3} \text{ Ohm} \cdot \text{cm}^2$. This is due to the formation of low-resistivity titanium silicides at the Si/Ti interface, which improves the contact properties. Ti can be replaced for other transition metals, such as Ni, Pd and Cr, since they also tend to form silicides after interaction with silicon.

The effect of RTA on the series resistance of diodes was studied for the example of p^+-n clamping diodes. It was shown that pulse treatment in an H_2 atmosphere at 340 °C for 20 s improved the series resistance and, as a result, increased the yield of multi-pad diodes by 15%. This confirmed the applicability of RTA for reducing the series resistance in silicon diode technology.

Furthermore, the effect of RTA on the reverse dark current was studied for the example of $p-i-n$ photocells based on highly ohmic p -Si with SiO_2 insulating film. It was shown that pulsed treatment in an H_2 atmosphere at 450 °C for 5 s improved the dark currents of the PP and the guard ring of the photocells and, as a result, increased the photodiode yield by 15%. This confirms the applicability of RTA in an H_2 atmosphere for reducing the dark currents in the technology of highly ohmic p -Si photodiodes due to the hydrogen saturation of dangling Si bonds, providing for a decrease in the density of the surface states and stabilization of the charge properties at the SiO_2/p -Si interface.

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