

Evaluating the effects of doping dynamics to unveiling the GaN MOSFET edge

P. Harikrishnan¹, P. Sivakumar¹

1 Department of Electronics and Communication Engineering, Kalasalingam Academy of Research and Education, Anand Nagar, Krishnankoil, Tamil Nadu, 626126, India

Corresponding authors: P. Harikrishnan (hari.k.p88@gmail.com) and P. Sivakumar (siva@klu.ac.in)

Received 19 September 2024 ♦ Accepted 2 March 2025 ♦ Published 16 July 2025

Citation: Harikrishnan P, Sivakumar P (2025) Evaluating the effects of doping dynamics to unveiling the GaN MOSFET edge. *Modern Electronic Materials* 11(2): 125–136. <https://doi.org/10.3897/j.moem.11.2.137432>

Abstract

This study presents a comparative performance analysis of GaAs, InP, and GaN-based MOSFETs using Spreading Resistance Profiling (SRP), Capacitance–Voltage (C–V) simulation, and Finite Element Analysis (FEA) within a sentaurus technology computer-aided design (TCAD) environment. The results show that GaN MOSFETs achieve the highest on-current (450 μ A) and peak gm (400 μ S), but exhibit a slightly higher ON-resistance (5 Ω) compared to GaAs (4.44 Ω) and InP (4.21 Ω). In terms of VTH uniformity, GaN demonstrates superior dopant stability with the lowest standard deviation (0.143 V), followed by InP (0.213 V) and GaAs (0.266 V). These findings highlight the trade-offs between current drive, resistance, and variability among III–V materials, with GaN offering strong performance and reliability characteristics suitable for secure and thermally stable semiconductor applications.

Keywords

gallium nitride (GaN), MOSFET, spreading resistance profiling (SRP), capacitance-voltage (C–V), finite element analysis (FEA), sentaurus technology computer-aided design (TCAD), III–V semiconductor device, dopant profile

1. Introduction

GaN MOSFETs, which are composed of gallium nitride and are metal-oxide-semiconductor field-effect transistors, are at the forefront of modern semiconductor technology and are heralding a new era of high-performance electronic devices. These devices have superior characteristics such as high electron mobility and robustness [1], making those key enablers for various applications, including power electronics and wireless communication systems [2, 3]. However, to fully utilize the potential of GaN MOSFETs and ensure their reliability in real-world scenarios, it is essential to gain a deeper understanding of their intricate material properties [4].

An important but often overlooked aspect that significantly affects the performance and reliability of GaN

MOSFETs is the dopant profile within the semiconductor material [5–7]. The dopant profile, which determines the distribution and concentration of dopants within the GaN lattice, has a profound influence on device behavior, including the threshold voltage, on-state resistance, and switching speed [8–9]. Therefore, the precise characterization of the dopant profile is crucial for unlocking the full potential of GaN MOSFET technology.

Simultaneously, as GaN MOSFETs are being widely adopted in industries with strict requirements for security and resilience, evaluating their susceptibility to tamper resistance, side-channel attacks, and thermal challenges has become increasingly important [10, 11]. Addressing these concerns requires an integrated approach that considers not only device performance but also security and thermal stability [3, 12].

In light of these considerations, our research aims to explore GaN MOSFETs from multiple perspectives, focusing on the interplay between dopant profile testing, device performance optimization, and real-world resilience. By utilizing advanced techniques, such as spreading resistance profiling (SRP) [13], capacitance-voltage (C-V) simulation [7], and finite element analysis (FEA), we aim to uncover new insights into the intricate dopant profiles of GaN MOSFETs and their implications for device behavior. Furthermore, our investigation extends beyond conventional performance metrics and includes assessments of security and thermal resilience. We aim to provide comprehensive insights into the reliability and safety of GaN MOSFETs by examining the dependencies between dopant profiles and device characteristics under different environmental conditions.

This research represents a pioneering effort to bridge the gap between fundamental material characterization, device performance optimization, and real-world applicability in GaN MOSFET technology. Through our multidimensional approach, we strive to push the boundaries of semiconductor research and pave the way for the next generation of high-performance and resilient electronic devices.

2. Literature survey

The evolution of GaN-based MOSFETs has gained significant momentum due to their exceptional electrical and thermal properties, positioning them as strong candidates for high-frequency and power device applications. R. Riedel and I.W. Chen [14] provided foundational insights into the material science of ceramics, including gallium-based compounds, which form the basis for GaN technology. Trapping phenomena, which often degrade GaN HEMT performance, have been thoroughly investigated by G. Meneghesso et al. [5], emphasizing the critical need for dopant control and transient stability. A detailed study by S. You et al. [15] highlighted process challenges and reliability limitations in vertical GaN devices, including thermal stress and etch-induced damage. R. Zhu et al. [16] proposed a step-graded channel doping technique in trench GaN MOSFETs to reduce leakage and improve breakdown characteristics, demonstrating the significance of vertical doping control.

Innovative device structures were further advanced by S. Chowdhury et al. [17], who patented a vertical GaN power FET with enhanced R_{on} and breakdown performance, confirming the benefits of trench engineering. N.K. Jaiswal and V.N. Ramakrishnan [18] proposed a reverse trench-gate architecture for DC-DC converters, achieving improved energy efficiency and current conduction. B.J. Baliga [1] earlier introduced a key figure of merit for high-frequency power devices, which remains relevant for comparing wide-bandgap devices like GaN, SiC, and GaAs. Recent reviews by C. Langpoklakpam et al. [2] detailed the fabrication and power handling

capabilities of vertical GaN MOSFETs, supporting further adoption in industrial environments. N. Islam et al. [3] comprehensively discussed the reliability, application landscape, and integration challenges of GaN HEMT devices, identifying current collapse and thermal fatigue as persistent limitations. The work of T. Oka et al. [19] demonstrated a vertical GaN trench MOSFET achieving 1.6 kV breakdown voltage on a native substrate, marking a significant leap in device blocking capabilities. I.C. Kizilyalli et al. [20] investigated long-term stress behavior and gate oxide degradation in GaN-on-GaN vertical structures, noting the importance of crystal quality and interface cleanliness. C. Liu et al. [21] addressed cost and compatibility concerns by proposing quasi-vertical GaN-on-Si MOSFETs, balancing performance and manufacturability. S. De Santi et al. [22] extended the discussion to GaN-based LEDs, analyzing physical mechanisms affecting reliability, including thermal stress and ion migration. F. Roccaforte et al. [4] presented a focused review on ion implantation in both SiC and GaN devices, illustrating challenges in achieving shallow, uniform junctions without defect generation.

Selective area regrowth, a promising technique for precision doping, was explored in detail by H. Fu et al. [9], who addressed interface contamination and crystal regrowth defects. N.K. Jaiswal and V.N. Ramakrishnan [23] introduced an optimized split-gate GaN trench MOSFET design for better switching performance and thermal resilience. M. Meneghini et al. [24] emphasized the physical origins of reliability issues in GaN devices and proposed modeling frameworks to predict failure under long-term stress. Y. Li et al. [12] further contributed by analyzing stepped doping structures in trench CAVETs, identifying key improvements in carrier confinement and breakdown control. Our own earlier work by P. Harikrishnan and P. Sivakumar [8] evaluated cubic boron arsenide (C-BAs) MOSFETs using TCAD for next-generation low-power applications, underlining the relevance of emerging compound semiconductors. H. Nan et al. [25] demonstrated surface modification of InSe nanosheets for better stability – relevant to doping and mobility control in layered semiconductors. A comparative study of advanced MOSFET concepts by C.H. Wann et al. [26] remains a valuable reference when benchmarking new transistor architectures. S. Verma et al. [27] proposed a doping-less GaN MOSFET structure, enhancing device reliability while simplifying fabrication. H. Fu et al. [9] provided a materials-level analysis of regrowth and doping strategies, identifying the trade-offs between selectivity and contamination risk.

J.P. Kozak et al. [6] presented a robust review of GaN device stability, thermal performance, and packaging challenges, which supports our current focus on threshold voltage uniformity. L. Nela et al. [10] explored multi-channel designs in GaN to increase drive current while maintaining short-channel control. K. Fu et al. [28] studied interfacial Si contamination during regrowth, showing its detrimental effect on vertical device

behavior. K. Jiang et al. [29] proposed a quantum-engineered *p*-doping method for ultra-wide bandgap nitrides, enabling deeper junction formation with less defect activation.

M. Buffolo et al. [11] reviewed the state-of-the-art in both GaN and SiC power device technology, including industrial trends and commercialization barriers. K. Ohnishi et al. [30] reported the fabrication of a *p*⁺-*n* vertical GaN diode using halide vapor phase epitaxy, achieving near-ideal avalanche behavior. S. Singh et al. [31] provided an overview of SiC and GaN technology evolution, highlighting ongoing material and fabrication breakthroughs. Y. Zhang et al. [32] reviewed GaN FinFET and tri-gate structures for RF and power applications, discussing the impact of 3D channel engineering. F. Roccaforte et al. [33] explored selective doping strategies for SiC, which are conceptually extendable to GaN doping control.

V. Sandeep et al. [34] presented a CSI-based analytical model for GaN MOS-HEMTs using high-*k* dielectrics, applicable to our analysis of capacitance-voltage behavior. D.W. Feldbaumer and D.K. Schroder [7] pioneered doping profiling in MOSFETs, laying the groundwork for the SRP techniques used in this study. S. Sharma et al. [13] recently proposed a source-drain resistance model for nanosheet FETs, relevant for modeling series resistance in compact GaN devices. Lastly, J. Zacharias et al. [35] introduced a novel suspended-gate FET sensor using polymer membranes, an emerging concept with potential crossover applications in GaN-based sensor integration.

3. GaN MOSFET technology

3.1. Fundamentals of Gallium nitride (GaN)

Gallium nitride (GaN) is a III-V compound semiconductor formed by combining gallium (group III) and nitrogen (group V) elements. GaN crystallizes in a wurtzite hexagonal structure, as shown in Fig. 1. Each Ga atom

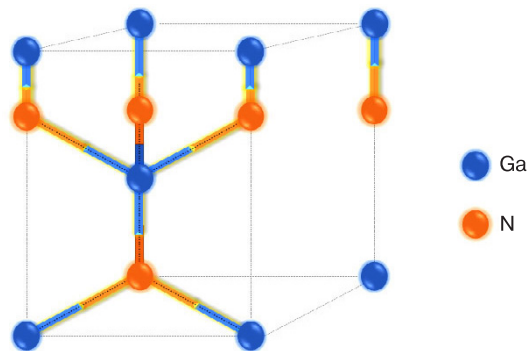


Figure 1. A wurtzite crystal structure of GaN [14]

contributes three valence electrons, while each N atom contributes five, forming strong covalent bonds. This robust crystal structure imparts GaN with a wide bandgap (~3.4 eV), high breakdown electric field (~3.3 MV/cm), and excellent thermal conductivity (~1.3 W/(cm·K)) [14].

These intrinsic properties make GaN suitable for high-power and high-frequency applications. Figure 2 compares key physical parameters such as bandgap, electron mobility, and thermal conductivity among GaN, GaAs, InP, and SiC. Notably, GaN offers a superior combination of wide bandgap and high electron saturation velocity, which enables faster switching and higher efficiency in power devices [5].

3.2. Gallium nitride metal oxide semiconductor

GaN-based MOSFETs represent a transformative leap in power semiconductor technology. These devices outperform traditional Si-based MOSFETs in voltage, frequency, and temperature endurance due to GaN's wide bandgap and high electron mobility (~2000 cm²/(V·s)) [15].

Figure 3a shows the structural overview of a GaN MOSFET, and Fig. 3b provides a cross-sectional view. The primary components include the GaN substrate, source, drain, gate, and gate oxide. Each plays a crucial role in device performance:

- **GaN substrate:** Acts as the base layer; its high critical electric field (~3.3 MV/cm) supports elevated breakdown voltages.
- **Source/Drain (S/D):** Enable electron injection and collection, respectively.
- **Gate (G):** Controls the conductive channel by modulating electric fields across the gate oxide.
- **Oxide layer:** Typically made from high-*κ* materials like Al₂O₃ or HfO₂, this insulator prevents gate leakage and enables high-speed switching.

The operational principle is similar to conventional MOSFETs: gate voltage modulates the conductive channel between source and drain. However, GaN devices can operate at frequencies >10 MHz and voltages >600 V with reduced on-resistance ($R_{on} < 50 \text{ m}\Omega\cdot\text{mm}$) [16, 17].

GaN MOSFETs are widely employed in applications such as:

- **Power converters:** High-efficiency DC-DC and AC-DC converters
- **RF systems:** Low-noise amplifiers and RF switches
- **Electric vehicles:** Onboard chargers and inverters

Their high-power density (>10 W/mm²) allows for compact and lightweight systems, critical in aerospace, automotive, and renewable energy sectors [18].

By replacing Si-based devices in high-power applications, GaN MOSFETs enable higher efficiency, lower thermal losses, and reduced cooling requirements. These attributes mark them as key enablers in next-generation electronic systems.

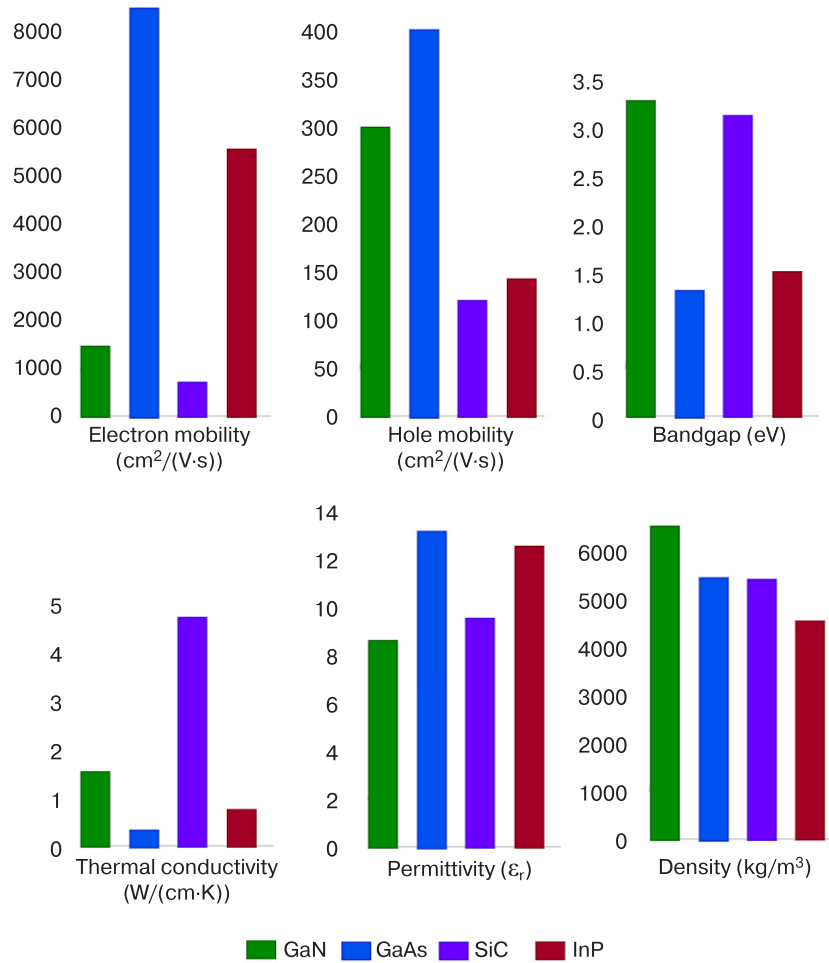


Figure 2. An overview of physical material parameters based on silicon carbide, germanium and gallium nitride [5, 14]

4. Dopant profile testing

4.1. Purpose of dopant testing

Dopant profile characterization is essential for validating the electrical behavior, reliability, and security of GaN MOSFETs. It ensures uniform charge carrier distribution, influences threshold voltage control, and mitigates adverse effects such as punch-through leakage, mobility degradation, and threshold voltage drift [7]. Moreover, dopant uniformity is vital for cryptographic applications where timing consistency and resistance to tampering are critical.

4.2. Techniques and methodology

Spreading resistance profiling (SRP) and finite element analysis (FEA) are combined to evaluate dopant behavior in GaN devices. SRP measures voltage drops under known current flow across microprobes in contact with the device surface, correlating resistance changes to dopant concentration [13]. This technique provides vertical profiling resolution on the order of tens of nanometers.

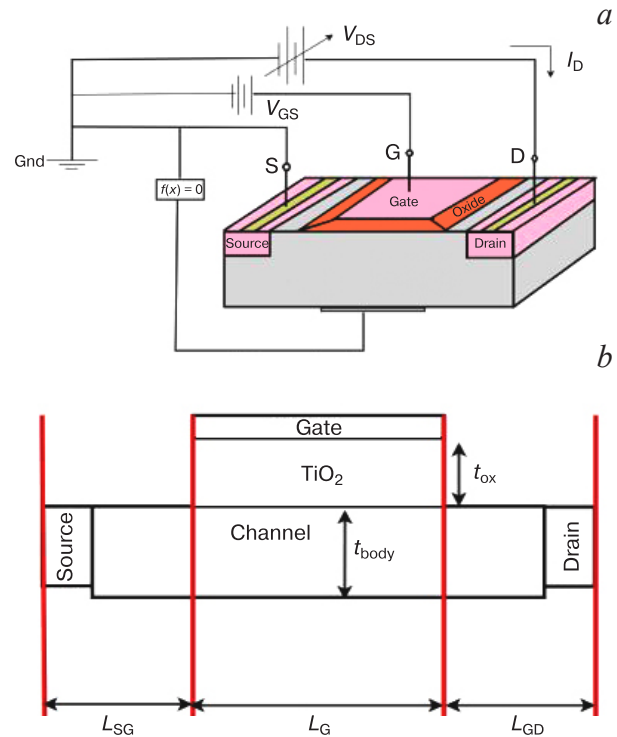


Figure 3. (a) GaN MOSFET, (b) a side view of a GaN substrate MOSFET

Finite element analysis is used to simulate electric potential and carrier transport using the Poisson and continuity equations under applied bias. Parameters such as dopant gradient steepness and junction depth are extracted and verified against SRP data. This hybrid approach supports accurate modeling of GaN MOSFET behavior across operating conditions and layout geometries.

4.3. Significance of GaN MOSFET

Precision in dopant profiling impacts several aspects:

- Ensures threshold voltage stability across operating temperatures.
- Detects anomalies from processing steps such as implantation damage.
- Supports design optimization for reduced short-channel effects.
- Assess doping-related variations that could be exploited in hardware security attacks.

As GaN devices scale down, maintaining tight control of doping profiles becomes essential for ensuring predictable electrical performance and long-term reliability.

5. Mode of dopant profile testing

5.1. Selection of GaN MOSFET samples and testing procedure

Figure 4 outlines the flowchart of the dopant profile testing methodology. Devices based on GaAs, InP, and GaN were chosen for benchmarking based on their contrasting bandgaps and mobility properties. SRP measurements were performed under room temperature (25 °C) using high-precision microprobes. The results were input into FEA simulations, developed in Sentaurus TCAD, which modeled dopant-dependent electric field distribution. Capacitance-voltage (C–V) analysis was conducted across a sweep of gate voltages to determine interface trap density, depletion width, and flat-band voltage. The combined use of SRP, FEA, and C–V profiling yields a comprehensive map of doping behavior and field effects across device architectures.

5.2. Experimental setup and conditions

Experimental setups were equipped with thermal stages to maintain test temperature stability within ± 0.5 °C. GaN MOSFETs were subjected to fixed drain bias while the gate voltage was modulated incrementally. Capacitance measurements were performed using an LCR meter with a 1 MHz test frequency. The test conditions mimicked real-world switching environments to assess device resilience. Data from SRP were cross-referenced with FEA-extracted profiles, ensuring fidelity in dopant gradient reconstruction. C–V-derived depletion region widths were used to validate built-in potential models and

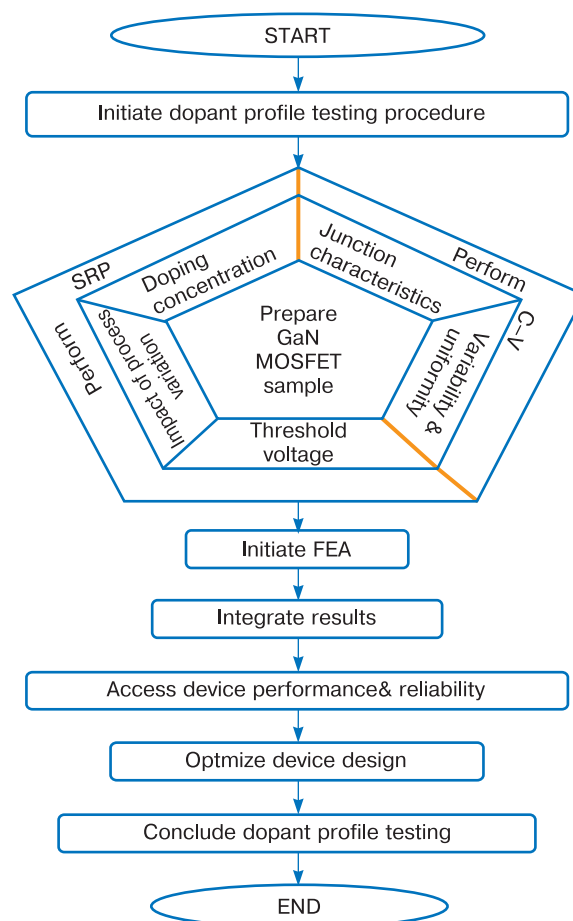


Figure 4. Flowchart of dopant profile testing

confirm doping depths. This approach ensures high-resolution, multidimensional evaluation of dopant effects in compound semiconductor MOSFETs.

6. Result and analysis

6.1. Presentation of dopant profile testing data

The combination of FEA and SRP offers a robust method for analyzing doping profiles in semiconductor devices, including dopant concentration, channel length, threshold voltage, and material parameters. FEA solves the Poisson equation, linking electric potential, charge density, and permittivity, to calculate the electric potential distribution and dopant concentration within device structures [35]. This enables comprehensive dopant profile simulations for materials like GaAs, InP, and GaN MOSFETs [16].

From Fig. 5, the output of MOSFETs made from GaAs, InP, and GaN by plotting the drain current (I_D) against the drain voltage (V_D) at a constant gate-source voltage ($V_{gs} = 2$ V) with running drain voltage (V_D). The GaN MOSFET, represented by the blue dashed line, exhibits the highest drain current among the three materials, reaching a saturation current (I_{on}) of approximately 450 μ A. This indicates

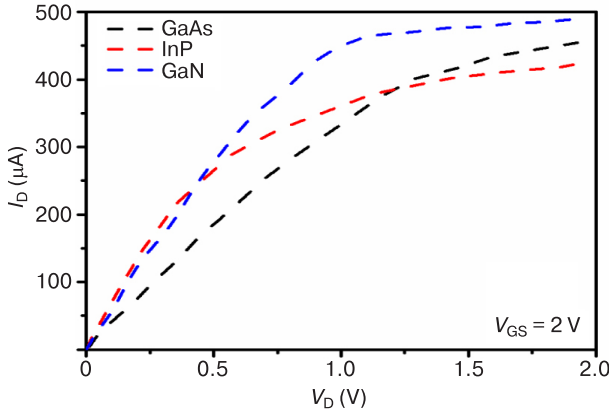


Figure 5. Drain current versus drain voltage of GaAs, InP and GaN substrate

that GaN has the best performance in terms of current conduction. The GaAs MOSFET, shown by the black dashed line, has a saturation current of about 400 μA , while the InP MOSFET, indicated by the red dashed line, reaches a saturation current of around 350 μA . These differences highlight the superior electron mobility and material properties of GaN compared to GaAs and InP, making GaN the best choice for achieving higher drive currents in MOSFET applications.

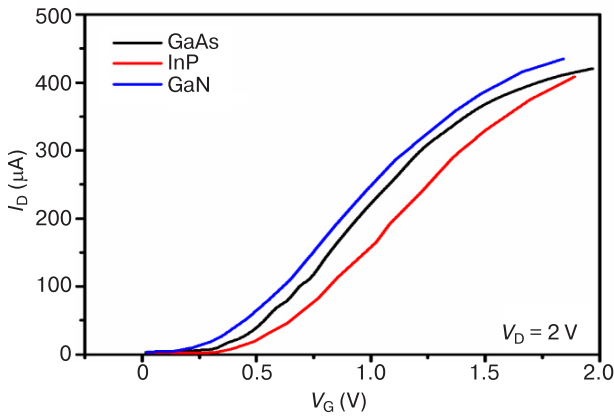


Figure 6. Drain current versus gate voltage of GaAs, InP and GaN substrate

Figure 6 compares the transfer characteristics of GaAs, InP, and GaN MOSFETs under a uniform drain voltage condition ($V_D = 2 \text{ V}$) with running gate voltage (V_G). The blue curve representing the GaN MOSFET demonstrates superior performance, with the highest on-state current (I_{on}) of approximately 475 μA and a reduced on-state resistance ($R_{\text{on}} \approx 4.21 \Omega$) compared to the other semiconductor materials. In contrast, the GaAs MOSFET showcases an on-state current of about 450 μA and an on-state resistance of roughly 4.44 Ω . Conversely, the InP MOSFET exhibits the lowest on-state current at around 400 μA and an on-state resistance of approximately 5 Ω . Remarkably, all three devices exhibit minimal off-state current (I_{off}) at a gate voltage of 0 V, resulting in notably high off-state resistance (R_{off}). This evaluation highlights the superior characteristics of GaN in achieving increased

current conduction and reduced on-state resistance, positioning it as the preferred choice for high-performance MOSFET applications. FEA is used to simulate complex physical systems with intricate geometries and varying conditions, offering insights into material and structural behavior under stress, strain, and temperature [35]. This helps improve designs and performance while reducing the need for costly prototypes, saving time and resources. Its integration with TCAD tools enhances analysis during the design phase. For compound semiconductors and MOSFETs, FEA is crucial in predicting device responses to electrical and thermal stresses, improving reliability and effectiveness [35]. Using first-order FEA for drain current vs. drain voltage and gate voltage, reliability is analyzed with Eqs (1) and (2).

$$A = \frac{h}{2} [f(a) + f(b)]; \quad (1)$$

$$\sum_{i=1}^n w f(x), \quad (2)$$

In Fig. 7 3D bar chart compares the FEA values for three semiconductor materials: GaN, GaAs, and InP. The x-axis represents the materials, the y-axis represents the electric field in V/m^2 , and the z-axis represents the FEA values in $I_D(\text{A})$. GaN demonstrates the highest FEA value of 3.0 A at an electric field of 1.5 V/m^2 . GaAs follows with an FEA value of 2.0 A at an electric field of 1.0 V/m^2 . InP shows the lowest FEA value of 1.0 A at an electric field of 0.5 V/m^2 . This chart highlights that GaN has the strongest field effect response, followed by GaAs and InP, under the specified electric field conditions.

The provided Fig. 8 illustrates the transfer characteristics (I_D vs V_G) and transconductance (g_m vs V_G) for MOSFETs utilizing GaAs, InP and GaN semiconductor materials, with a constant drain voltage ($V_D = 2 \text{ V}$) and a gate length (L_G) of 200 nm.

The GaAs MOSFET (black line) demonstrates a steady increase in drain current (I_D) with increasing gate voltage (V_G), peaking at around 400 μA . Its transconductance (g_m) also increases to a maximum

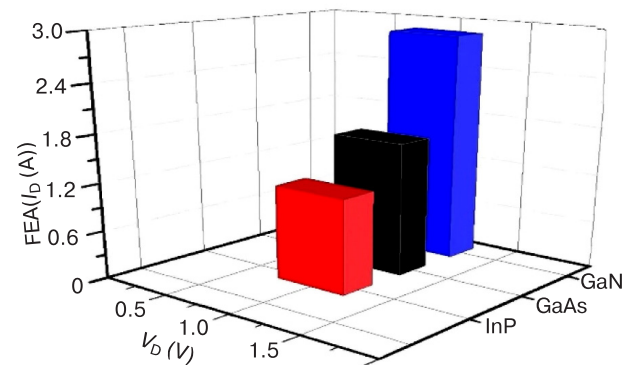


Figure 7. FEA of drain current versus drain voltage of GaAs, InP and GaN substrate from Fig. 5

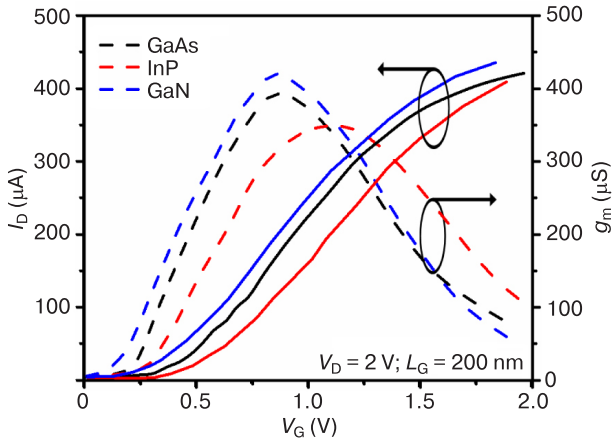


Figure 8. Drain current versus gate voltage versus transconductance of GaAs, InP and GaN substrate

Table 1. Observed values of compound semiconductor materials

Result	GaAs	InP	GaN
I_{on} (μA)	400	350	450
R_{on} (Ω)	4.44	4.21	5
Peak transconductance (μS)	350	300	400

value of approximately 350 μS before declining. The InP MOSFET (red line) similarly shows an increase in drain current with gate voltage, reaching a peak of approximately 350 μA , while its peak transconductance is around 300 μS . The GaN MOSFET (blue line), however, outperforms both GaAs and InP MOSFETs by achieving the highest peak drain current of around 450 μA and a peak transconductance of approximately 400 μS . These values are tabled in Table 1 as shown in below.

6.2. Junction characteristics by C–V test

Figure 9 explains a Colpitts oscillator circuit using a GaN MOSFET, known for its efficiency and high-frequency

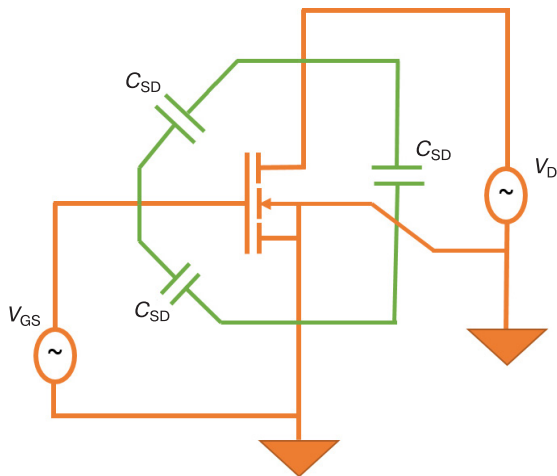


Figure 9. Small-signal diagram of the GaN MOSFET capacitance vs voltage

performance. In this circuit, the GaN MOSFET acts as the active component, with two capacitors in series forming part of the resonant tank circuit, coupled with an inductor. This LC circuit determines the oscillation frequency. The feedback for sustaining oscillations is provided by the capacitors' voltage division, sending a portion of the output signal back to the MOSFET's gate. AC voltage sources are included: one for initiating oscillation at the gate and the other for delivering the output via the drain. Ground connections ensure stability, generating a consistent high-frequency signal utilizing the GaN MOSFET's capabilities. The Eq. (3) representing the built-in potential (V_{bi}) is a crucial parameter in the context of a MOSFET based on a GaAs, InP and GaN substrate, serving as a quantitative indicator of the potential variance across the junction established between the gate oxide and the graphene channel.

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_D N_A}{n_i^2} \right), \quad (3)$$

where V_{bi} is built-in potential of the junction, $k = 1.38 \cdot 10^{-23}$ J/K (Boltzmann constant), $T = 298$ K (temperature in Kelvin), $q = 1.6 \cdot 10^{-19}$ C (electron charge), N_D is the donor concentration, N_A is the acceptor concentration, n_i is intrinsic carrier concentration

The built-in potential (V_{bi}) is crucial for several reasons. First, it creates equilibrium in the MOSFET, preventing further charge carrier diffusion and ensuring stable device operation. This equilibrium is essential for proper functionality. Second, V_{bi} directly impacts the threshold voltage (V_{th}), the minimum gate voltage needed to invert the semiconductor surface and form a conductive channel between the source and drain. Additionally, the built-in potential affects the C–V characteristics [7], which are important for understanding gate capacitance and switching behavior. This helps engineers optimize doping levels and material properties for better electrical efficiency, enhancing device configuration for specific applications. A well-defined V_{bi} also reduces short-channel effects in smaller MOSFETs, improving switching speeds and power efficiency for high-performance applications

$$w = \sqrt{\frac{2\epsilon_s (V_{bi} - V_{gs})}{q N_D}}, \quad (4)$$

where, w is depletion width in the semiconductor, ϵ_s is permittivity of the semiconductor material, V_{bi} is built-in potential of the junction, V_{gs} is gate-to-source voltage, $q = 1.6 \cdot 10^{-19}$ C (electron charge), N_D is donor concentration, representing the concentration of donor atoms in the n -type semiconductor region.

The calculation of the depletion width w in the semiconductor region of a MOSFET is determined by a specific Eq. (4). This equation is formulated based on Poisson's equation, which establishes a relationship between the charge density and the electric field within a semiconductor. The depletion width signifies the area in

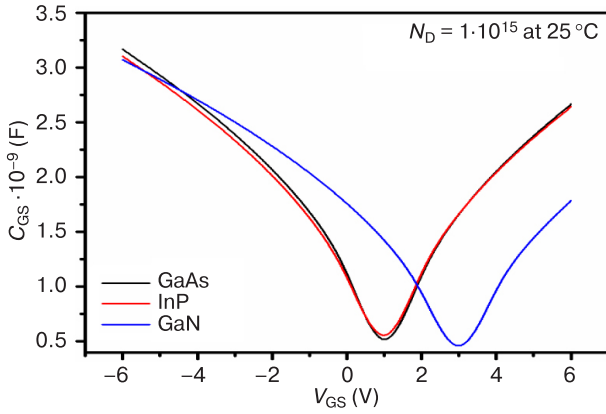


Figure 10. Gate capacitance versus gate voltage of GaAs, InP and GaN substrate

the semiconductor where there is a reduction in mobile charge carriers due to the presence of an applied electric field.

Figure 10 shows the variation of the gate-source capacitance (C_{gs}) as a function of gate-source voltage (V_{gs}) for three different semiconductor materials: GaAs, InP, and GaN, at a doping concentration (N_D) of $1 \cdot 10^{15}$ at 25°C . The curves indicate that C_{gs} changes with V_{gs} for each material, demonstrating a distinct minimum point. GaAs and InP exhibit similar capacitance profiles, with capacitance decreasing to a minimum around 0 before increasing symmetrically. In contrast, GaN shows a wider and more pronounced minimum, indicating a different capacitance behavior and potentially higher sensitivity to V_{gs} changes, which can be advantageous in high-frequency and high-power applications

$$c_d = \frac{\epsilon_s}{w}. \quad (5)$$

In a MOSFET, the formation of the depletion region occurs upon the application of a voltage to the gate terminal. This results in the generation of an electric field that causes a reduction in the number of free charge carriers near the interface between the semiconductor and oxide layers. From Eq. (5), the depletion capacitance (C_D) emerges from this specific region and exhibits an inverse

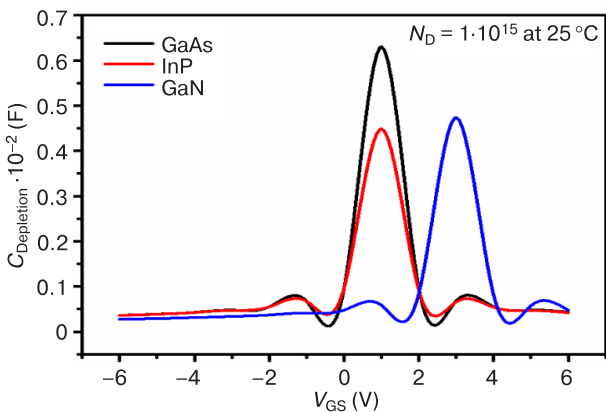


Figure 11. Depletion capacitance versus gate voltage of GaAs, InP and GaN substrate

relationship with the width (w) of the depletion region. For smaller values of w , the depletion region tends to be narrower, leading to a higher value of capacitance C_D . Conversely, when w is increased, the depletion region widens, resulting in a decrease in the capacitance C_D . Understanding this correlation is essential for comprehending the impact of gate voltage on the behavior of the MOSFET, particularly within the threshold region where the device transitions between the off-state and the on-state. The depletion capacitance plays a significant role in determining the total capacitance observed at the gate, thereby influencing the switching characteristics and frequency response of the MOSFET.

The Fig. 11 illustrates the correlation between depletion capacitance (C_D) and gate-source voltage (V_{gs}) for three distinct semiconductor materials: GaAs, InP, and GaN, at a doping concentration (N_D) of $1 \cdot 10^{15}$ at 25°C . The plotted curves demonstrate the variation of depletion capacitance in response to the applied gate-source voltage for each material. GaAs and InP exhibit similar trends, characterized by sharp capacitance peaks at specific V_{GS} levels, indicating regions of rapid depletion width alteration. Conversely, GaN displays a broader and less prominent peak, implying a contrasting capacitance behavior and depletion region reaction to the gate voltage. This disparity in capacitance attributes is a manifestation of the unique material characteristics of GaN, which could potentially impact its efficacy in applications involving high-frequency and high-power scenarios in comparison to GaAs and InP.

6.3. Variability and uniformity testing data

Variability and uniformity testing in MOSFETs are essential for ensuring consistent performance across manufacturing batches and wafers [7]. Key tests focus on V_{th} and g_m across different gate lengths, potential variations, and dopant concentrations. V_{th} testing measures how changes in gate length, potential, and doping affect V_{th} , helping manage short-channel effects and electrical stress. Consistent V_{th} under varying conditions indicates stable manufacturing and effective doping control. Parameter g_m testing measures the change in drain current with gate voltage, assessing the device's amplification capacity. Analyzing g_m under different conditions ensures uniform amplification and reveals the stability of the manufacturing process. Testing V_{th} and g_m ensures minimal variability and high consistency, improving the reliability and performance of MOSFETs in integrated circuits.

$$V_{th} = V_{fb} + 2\phi_F + \frac{Q_D}{C_{ox}}; \quad (6)$$

$$\phi_F = \frac{kT}{q} \ln \left[\frac{N_A}{n_i} \right]; \quad (7)$$

$$Q_D = qN_A x_d T; \quad (8)$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}, \quad (9)$$

where V_{th} is threshold voltage, V_{fb} is flat band voltage, ϕ_F is potential difference, Q_D is charge in the depletion region, C_{ox} is gate oxide capacitance, k is Boltz man constant, T is temperature, N_A is dopant concentration and n_i is intrinsic carrier concentration, x_d is maximum depletion width (cm), ϵ_{ox} is permittivity of oxide and t_{ox} is oxide thickness (cm).

From Eqs (6)–(9) the threshold voltage (V_{th}) of a MOSFET is defined as the minimum gate-source voltage required to establish a conductive channel between the source and drain terminals. This threshold voltage is influenced by various factors: the flat-band voltage (V_{fb}), which compensates for disparities in work function between the gate material and the semiconductor; twice the Fermi potential ($2\phi_F$), which guarantees that the surface potential is adequate to induce inversion in the semiconductor surface and create a conductive channel; and the term Q_D , C_{ox} , which denotes the extra gate voltage necessary to equalize the charge in the depletion region (Q_D) with the induced charge on the gate, where C_{ox} represents the capacitance of the gate oxide layer. Collectively, these factors ascertain the gate voltage required to activate the

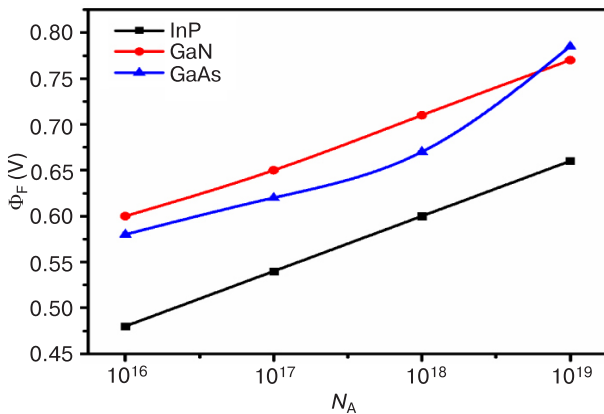


Figure 12. Potential difference versus dopant concentration of GaAs, InP and GaN substrate

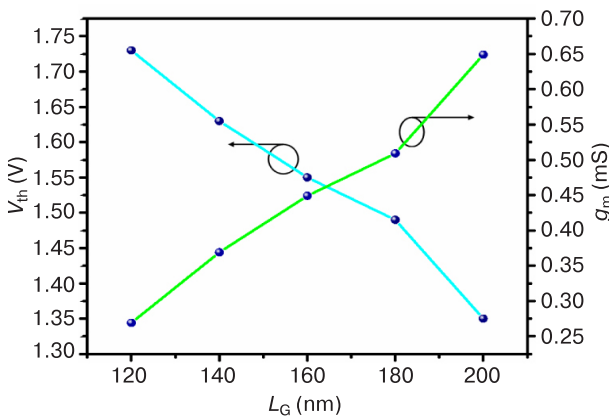


Figure 13. Threshold voltage and transconductance with varying gate length of GaN substrate

MOSFET, underscoring the significance of this equation in comprehending and formulating MOSFET devices.

The Fig. 12 illustrates the relationship between the Fermi potential (Φ_F) and the acceptor concentration (N_A) for three semiconductor materials: InP, GaN, and GaAs. The x -axis represents the acceptor concentration (N_A) on a logarithmic scale ranging from $1 \cdot 10^{16}$ to $1 \cdot 10^{19}$ cm⁻³, while the y -axis shows the Fermi potential (Φ_F) in volts (V), ranging from 0.45 to 0.80 V. The data points for InP, GaN, and GaAs are represented by black squares, red circles, and blue triangles, respectively. For InP, the Fermi potential increases linearly with the acceptor concentration, starting around 0.50 V at $N_A = 1 \cdot 10^{16}$ cm⁻³ and reaching approximately 0.65 V at $N_A = 1 \cdot 10^{19}$ cm⁻³. GaN exhibits a more rapid increase, with the Fermi potential starting around 0.55 V at $N_A = 1 \cdot 10^{16}$ cm⁻³ and reaching about 0.75 V at $N_A = 1 \cdot 10^{19}$ cm⁻³. GaAs shows an intermediate behavior, with the Fermi potential starting around 0.60 V at $N_A = 1 \cdot 10^{16}$ cm⁻³ and reaching approximately 0.78 V at $N_A = 1 \cdot 10^{19}$ cm⁻³. These observations indicate that GaN has the highest increase in Fermi potential with increasing acceptor concentration, making it more sensitive to doping levels compared to InP and GaAs. This data is crucial for optimizing the electrical properties of semiconductor devices.

The Fig. 13 illustrates the relationship between the gate length (L_G) of a MOSFET and two key parameters: V_{th} and g_m . The x -axis represents the gate length (L_G) in nanometers (nm), ranging from 120 to 200 nm. The left y -axis shows the V_{th} in volts (V), ranging from 1.30 to 1.75 V, while the right y -axis indicates the g_m in mS, ranging from 0.25 to 0.70 mS. The cyan line depicts the threshold voltage, which decreases with increasing gate length, starting at approximately 1.75 V for a gate length of 120 nm and dropping to around 1.35 V for a gate length of 200 nm. Conversely, the green line represents the transconductance, which increases with gate length, starting at about 0.30 mS for a gate length of 120 nm and rising to around 0.65 mS for a gate length of 200 nm. This Fig. 13 highlights the inverse relationship between the threshold voltage and transconductance concerning the gate length. As the gate length increases, the threshold voltage decreases, indicating a lower voltage required to turn on the MOSFET, while the transconductance increases, reflecting an improved ability of the MOSFET to control the output current. The intersections and marked circles on the graph suggest points of particular interest

Table 2. Observed variability and uniformity of V_{th} by varying L_G

Material	Mean threshold voltage (V)	Standard deviation for uniformity of V_{th} (V)
GaAs	1.43	0.266
InP	1.12	0.213
GaN	1.55	0.143

or significant changes in the trends, crucial for optimizing MOSFET performance in various applications.

The Table 2 describes the distinct properties of GaAs, InP, and GaN regarding their threshold voltages and consistency. GaN emerges as the most notable due to its highest average V_{th} and the least standard deviation, rendering it well-suited for applications requiring high power and high uniformity. InP, on the other hand, presents the lowest average V_{th} , making it appropriate for low-power applications, albeit with moderate consistency. In contrast, GaAs exhibits a high average V_{th} but displays more variability, necessitating stricter control during the manufacturing process to ensure reliable performance.

7. Conclusion

This study presented a detailed investigation of GaN MOSFETs using advanced dopant profiling techniques, including Spreading Resistance Profiling (SRP), Capacitance-Voltage (C-V) characterization, and Finite Element Analysis (FEA) simulations within a TCAD framework. We aimed to analyze the relationship between dopant profile variations and critical device parameters such as threshold voltage V_{th} , g_m , and field-effect behavior. Our findings revealed that GaN devices demonstrated superior threshold voltage stability (mean $V_{th} = 1.55$ V, $\sigma = 0.143$ V), higher I_D (~ 450 μ A), and peak g_m (~ 400 μ S), outperforming GaAs and InP alternatives. FEA simulations and C-V measurements further confirmed GaN's broader depletion regions, improved gate control, and lower on-state resistance (~ 4.21 Ω), all of which are favorable for high-frequency switching applications. In addition to electrical performance, our analysis addressed security-related considerations by validating dopant uniformity and resistance to variability, both of which are critical in secure electronics. The integration of TCAD tools ensured the reproducibility of these findings under variable device and environmental conditions.

In summary, this research validates the use of GaN as a high-performance, thermally stable, and secure material

platform for next-generation power and RF electronics. The hybrid methodology demonstrated here provides a model for future studies aiming to optimize doping strategies and reliability in wide-bandgap semiconductor technologies.

8. Future work

Efforts will focus on improving the thermal stability and security of GaN MOSFETs by optimizing dopant profiles. Advanced simulations and experimental validations will refine device architecture to reduce side-channel vulnerabilities and enhance tamper resistance. Exploration of GaN MOSFET integration with materials like graphene will seek synergistic effects to boost performance and reliability. Extended-term reliability testing in various conditions will ensure device longevity. Innovation in fabrication techniques will aim for precise doping control, enhancing device performance. Future research will advance GaN MOSFET technology, supporting its adoption in high-performance, secure electronic applications.

Acknowledgement

The authors express their gratitude for the assistance provided by Kalasalingam Academy of Research and Education (KARE) in the form of a fellowship grant and access to TCAD facilities. Their profound appreciation extends to the VLSI Research Lab for their indispensable resources that greatly contributed to the research endeavor. Moreover, they wish to express their gratitude to the Center of VLSI for their support in utilizing the TCAD laboratory facilities, which played a key role in the successful completion of the study.

Conflict of interest

Author has declared no conflict of interest.

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